AMENDMENTS

In the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application.

1. (Currently Amended) An ATM switching equipment comprising:

a switching network;

an input interface unit including an input processing unit;

an output interface unit including an output processing unit;

a microprocessor;

a server switching unit comprising:

an AAL2 switcher that is connected to the switching network via a first interface;

an input processing unit to which said AAL2 switcher is connected; and

an output processing unit to which said AAL2 switcher is connected;

said switching equipment being configured to write a new VPI/VCI information, including VPI/VCI bits, for a further connecting section into cells of arriving data streams upon utilization of routing tables,

said AAL2 switcher being configured for simultaneous processing of a maximum plurality of incoming connections, an AAL2 routing list being provided for each of said incoming connections;

said AAL2 switcher being connected to said switching network without requiring recognition of all VPI/VCI bits in the AAL2 switcher; and

said microprocessor limiting the number of bits representing VPI/VCI bits from among VPI/VCI bits transmitted in a header of ATM cells to be interpreted according to a number of ATM connections ~~capable of being processed~~ available for processing as indicated in said AAL2 routing lists, so that said first interface considers corresponding VPI/VCI bits.

2. (Previously Presented) The ATM switching equipment according to claim 1, wherein said first interface is a UTOPIA interface.

3. (Previously Presented) The ATM switching equipment according to claim l, wherein a single virtual path is established between said switching network and said server switching unit.

4. (Previously Presented) The ATM switching equipment according to claim 1, further comprising:

buffer memories which are allocated to said routing lists; and

a section of an AAL2 packet of an ATM cell being writable into said buffer memories,

said section being readable from said buffer memories when processing a next-successive ATM cell and for completion of a remainder of said AAL2 packet.